325714(28)

B. E. (Seventh Semester) Examination, Nov.-Dec. 2015

(Old Scheme)

(EEE Branch)

ADVANCED ELECTRONIC CIRCUITS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Attempt all the questions with internal choice. Part 'a' is compulsory & attempt any two parts out of 'b', 'c' or 'd'. Assume suitable data whenever required. Symbols used have their usual meaning.

1. (a) What is "Aperture Time" in conjunction with Digital to Analog (D/A) conversion. 2

(b) Discuss successive approximation ADC with complete

discription of block diagram. Explain conversion process giving some example. 7

(c) Design a 3 bit digital to analog conversion that accepts 2's complement formatted input and provide the output in the range of – 4 volts to +3 volts. 7

(d) Explain specifications of D/A converter : 7

(i) Resolution

(ii) Linearity

(iii) Accuracy

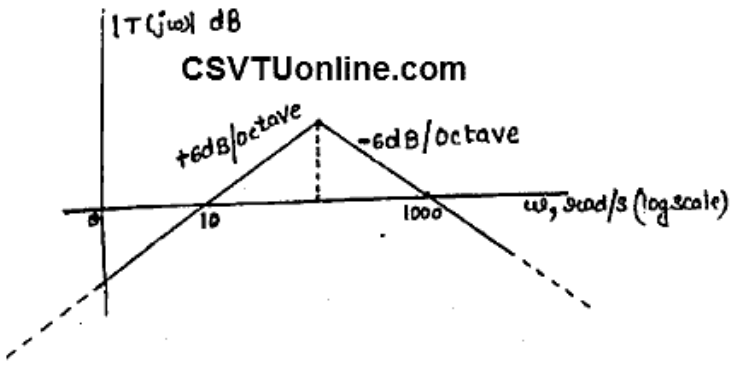
(iv) Settling Time

(v) Temperature sensitivity

2. (a) Define Bi-linear transfer function. 2

(b) Explain with circuit diagram the Tour-Thomas Biquad-circuit. What are the steps of the tunning algorithm? 7

(c) Design a bandpass filter having the asymtotic Bode plot shown in figure below. Use a minimum number of opamps in your realization. Scale element values until they are in a partical range. 7

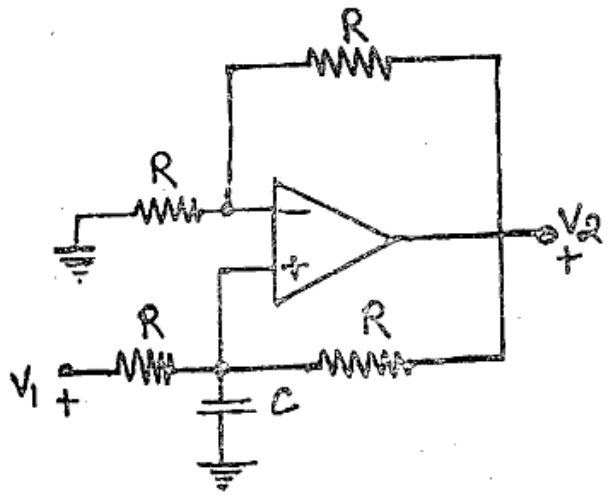


7

(d) For the circuit shown in fig.-below, show that

$$\frac{V_2}{V_1} = \frac{2}{RCs}$$

show that the use of this circuit in the biquad circuit permits us to reduce the number of opamps required to two. CSVTUonline.com 7



3. (a) Define sensitivity of the filter and give its expression. 2

(b) Explain with circuit diagram the working of sallen key circuits. CSVTUonline.com 7

(c) Consider sallen-key low pass circuit for $k = 1$ which is to be designed to realize a pair of poles located at the angles $\pm\psi$ with respect to negative real axis of s-plane, If $R_1 = R_2 = 1$, show that

$$\cos\psi = \sqrt{\frac{c_2}{c_1}} = \left(\frac{c_2}{c_1}\right)^{1/2}.$$ 7

(d) Explain the stagger tuned band pass filter design steps. 7

4. (a) List the basic building blocks of a PLL. 2

(b) What are the different types of digital phase detector? Explain. CSVTUonline.com 7

(c) Derive expression for lock range and capture range of PLL. 7

(d) Explain with proper block diagram principle of operation of VCO. 7

5. (a) What do you mean by "Feed through" in terms of analog multiplier. 2

(b) Explain four quadrant multiplier circuit using RC 4200 along with circuit diagrams and expression for the output. 7

(c) Explain any three applications of multiplier circuits. 7

(d) An analog multiplier has a 3-dB bnd width of 50 MHz. Find the freq. at which this limited bandwidth will result in a multiplication errors of 0·1%. 7