Printed Pages : 3

Roll No.

328551(28)

BE (5th Semester)
Examination, Nov.-Dec., 2018

(New Scheme)

Linear Integrated Circuits
&
Applications

Time Allowed : 3 hours *Maximum Marks* : 80

Minimum Pass Marks : 28

Note : (*i*) Attempt any **two** parts from (*b*), (*c*) and (*d*) of each question. Part (*a*) is compulsory in each question.

(*ii*) The figures in the right-hand margin indicate marks.

1. (*a*) Define slew rate. [2]

(*b*) Discuss the characteristics of an ideal operational amplifier. [7]

(*c*) For dual input, balanced output differential amplifier, show that output voltage gain, $A_d = \frac{R_c}{r_e}$, using *r*-parameter analysis (where R_c is collector resistance and r_e is a.c. emitter resistance). [7]

(*d*) Explain block diagram of typical operational amplifier. [7]

2. (*a*) What is voltage follower? Draw its circuit diagram. [2]

(*b*) Design the op-amp circuit which can give output as $V_o = 2\ V_1 - 3V_2 + 4V_3 - 5V_4$. [7]

(*c*) Design a Schmitt trigger circuit using operational amplifier. Explain operation of this circuit. [7]

(*d*) Design a practical integrator with a d.c. gain of 10, to integrate a square wave of 10 kHz. [7]

3. (*a*) What are important steps in analog to digital conversion? [2]

(*b*) Explain dual-slope ADC with its functional block diagram. [7]

(*c*) Explain the *R*-2*R* ladder technique for digital to analog conversion for digital input 011. Also give its advantage over binary weighted resistor type. [7]

(*d*) What are the important specifications of Digital to Analog Converters? [7]

4. (*a*) Define voltage regulator [2]

(*b*) Differentiate between series and shunt voltage regulators, using op-amp. [7]

(*c*) Explain internal structure of IC 723. [7]

(*d*) Explain characteristics of voltage regulators. [7]

5. (*a*) Define capture range. [2]

(*b*) Discuss the application of PLL circuit as frequency synthesizer. [7]

(*c*) Write and explain an application of multiplier circuit. [7]

(*d*) Draw the block schematic of PLL and explain its working principle. [7]

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