BE (3rd Semester)
Examination, Nov.-Dec., 2018

(New Scheme)

Digital Logic Design

Time Allowed : 3 hours | *Maximum Marks :* 80
Minimum Pass Marks : 28

Note : (*i*) Attempt **all** questions. Part (*a*) of each question is compulsory. Attempt any **two** parts from (*b*), (*c*) and (*d*) of each question. Assume suitable data wherever necessary.

(*ii*) The figures in the right-hand margin indicate marks.

1. (*a*) What is self-complementing code? [2]

(*b*) (*i*) Convert the Gray code 1101 to binary.

(*ii*) Convert $3A7_{16}$ into Gray number.

(*iii*) In an even-parity scheme, which of the following words contain an error?

(*m*) 10101010, (*n*) 11110110, (*p*) 10111001

(*iv*) Encode data bits 1101 into the 7-bit even-parity Hamming code. [7]

(*c*) (*i*) Reduce the expression

$$f = A + B\left[AC + (B + \bar{C})D\right]$$

(*ii*) Show that

$$A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$$ [7]

(*d*) Realize the X-OR function, i.e.

$X = A\bar{B} + \bar{A}B$ using NAND logic and NOR logic. [7]

2. (*a*) What are "don't care" combinations? [2]

(*b*) Minimize the following using K-map : [7]

(*i*) $F(w, x, y, z) = \Sigma m(1, 3, 7, 11, 15) + \Sigma d(0, 2, 5)$

(*ii*) $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 4, 5) + d(10, 11, 12, 13, 14, 15)$ in POS form.

(*c*) Using the tabular method, obtain the minimal expression for

$F(A, B, C, D) = \Sigma m(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$ [7]

(*d*) Give the comparison between PROM, PLA and PAL. [7]

3. (*a*) Compare a decoder with a demultiplexer. [2]

(*b*) What is the difference between serial adder and parallel adder? Briefly explain the serial adder with logic diagram. [7]

(*c*) With the help of a logic diagram and a truth table, explain an octal-to-binary encoder. [7]

(c) Implement the following function with a MUX :

$$F(a, b, c) = \Sigma m\,(1, 3, 5, 6)$$

Choose a and b as select inputs. [7]

4. (a) What is meant by race-around condition in flip-flops? [2]

(b) Draw a circuit diagram of a master-slave J-K flip-flop and explain its operation with the help of a truth table. How it is different from edge triggering? Explain. [7]

(c) What is the basic difference between a shift register and a counter? With neat diagram, explain the working of a 4-bit universal shift register. [7]

(d) Design a 3-bit synchronous up counter. [7]

5. (a) Define Fan-in and Fan-out. [2]

(b) With the help of a neat diagram, explain the working of a two-input TTL NAND gate. [7]

(c) What are the merits and demerits of TTL, ECL and CMOS? [7]

(d) Write short notes on interfacing of various logic families. [7]

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