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322454(22)

BE (4th Semester)
Examination, April - May, 2017

[New Scheme]

Computer Systems Architecture

Time Allowed : 3 hours *Maximum Marks :* 80
Minimum Pass Marks : 28

Note : (*i*) Part (*a*) of each question is compulsory. Attempt any **two** parts from (*b*), (*c*) and (*d*) of each question.

(*ii*) The figures in the right-hand margin indicate marks.

UNIT - I

1. (*a*) Define the concept of Bit slice. [2]

(*b*) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200.

Evaluate the effective address if the addressing mode of the instruction is

(*i*) Direct

(*ii*) Immediate

(*iii*) Relative

(*iv*) Register Indirect [2+2+2+1]

(*c*) Explain the working of a Typical Hardwired control unit and differentiate it from micro programmed control unit. [7]

(*d*) Convert the following arithmetic expressions from infix to reverse polish notation :

(*i*) A*B + C*D + E*F [3½]

(*ii*) A+B * [C*D + E* (F + G)] [3½]

UNIT - II

2. (*a*) What do you mean by Divide Overflow Condition? [2]

(*b*) Show step-by-step multiplication process using Booth algorithm. Assume 5-bit registers that hold signed numbers
(–9) × (–13). [7]

(*c*) Show the contents of registers E, A, Q and SC during the process of division of 10100011 by 1011 using Restoring method. [7]

(*d*) Explain the working of carry look ahead adder with a neat diagram. [7]

UNIT - III

3. (*a*) What is the need of multilevel memory hierarchy? [2]

(*b*) Explain the working of an associative memory with neat diagram. [7]

(*c*) The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent of the memory requests are for read and remaining 20 percent for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.

(*i*) What is the average access time of the system considering only memory read cycles? [3]

(*ii*) What is the average access time of the system for both read and write requests? [2]

(*iii*) What is the hit ratio taking into consideration the write cycles? [2]

(*d*) Write short notes on the following :

(*i*) Virtual memory [3½]

(*ii*) Cache memory [3½]

UNIT - IV

4. (*a*) Define Interrupt. [2]

(*b*) Explain the working of DMA (Direct Memory Access) with a neat diagram. [7]

(*c*) Explain asynchronous data transfer and also differentiate it from synchronous data transfer. [7]

(*d*) Write short notes on the following :

(*i*) Daisy chaining priority [3½]

(*ii*) Parallel priority interrupt [3½]

UNIT - V

5. (*a*) What do you understand by parallel processing? [2]

(*b*) Differentiate between instruction pipeline and arithmetic pipeline (with example). [7]

(*c*) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks. [7]

(*d*) Write short notes on the following :

(*i*) Data dependency [3½]

(*ii*) Array processors [3½]