(4)

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Unit - V

5.	(a)	80386 microprocessor is highly pipelined as compared with 8086 microprocessor. Justify.	2
	(b)	Discuss the architecture of 80386 and explain the function of each unit.	7
	(c)	Differentiate between real mode, virtual mode and protected mode of 8086.	7
	(d)	What do you mean by descriptor table? Discuss different descriptor types supported by 80386.	7
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BE (5th Semester) Examination, Nov.-Dec., 2015

(New Scheme)

ETC

Advanced Microprocessor and Interfacing CSVTUonline.com

Time Allowed: 3 hours Maximum Marks: 80
Minimum Pass Marks: 28

Note: (i) Part (a) of each question is compulsory.

Attempt any two parts from (b), (c) and (d).

(ii) The figures in the right-hand margin indicate marks.

Unit - I

(a) Draw and label Flag Register Organization of Intel 8086.
(b) Explain the pipelined architecture of 8086 with block diagram. How is it implemented in 8086?
(c) Explain the concept of segmented memory. What are its advantages?
(d) Draw and discuss read and write timing diagram with one wait state of 8086 in

TC-206

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minimum mode.

(Turn Over)

7

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(b) i d		Unit - II Why 8086 microprocessor is not having any opcode fetch cycle? Explain the interrupt structure of 8086 in detail with interrupt vector table. Also calculate the interrupt vector address of the following interrupt:	2		(d)	generate a square wave of period 1 ms. The 8086 and 8254 run at 6 MHz and 1.5 MHz respectively. Explain the initialization sequence of	7
		(i) INT OH	·			8259 A. CSVTUonline.com	
		(ii) INT 20H CSVTUonline.com	-			Unit - IV	
	(4) What are the different addressing modes supported by 8086? Give one example for		4.	(a)	Why are converters used? Write application of ADC and ADC.	2
		each of them.	7.		(6)	Explain Stepper Motor Interfacing.	7
	(d	Write a program to find out the number of even and odd numbers from a series of 16-bit hexadecimal numbers. Assume any 10 hexadecimal numbers.	7	(<i>c</i>)	Interface ADC 0808 with 8086 using 8255 ports. Use port A of 8255 for		
		Unit - III . CSVTUonline.com				the CPII and port C for control signals.	
3.	(a)	What is the main difference between 8259 and 8259A? Interface two 4K×8 EPROMs and two 4K×8 RAM chips with 8086 and select suitable maps. The address ranges are defined	2		Assume that an analog input is present at 1/P ₂ of the ADC and a clock input of suitable frequency is available for ADC. Write required ALD and draw schematic	7	
						diagram. CSVTUonline.com	•
((c)	EPROM → FEOOO H - FFFFF H RAM → FCOOO H - FDFFF H Design a programmable times using 8254 and 8086. Interface 8254 at an address 0040 H for counter 0 and write an ALP to	7		(d)	Explain the following terms in relation to 8279:	7
	((i) Two-Key Lock Out (ii) N-Key Roll Over	
TC-2	06	an ALP to					
		(Continue		Ø		(iii) Right Entry	
						(iv) Left Entry	