BE (Forth Semester)

Electrical And Electronics Engineering

Digital Electronics and Logical Design - 325456(25)

2014 - Winter Session , New Scheme

Chapter 1

1	Realize the logic expression : \(Y = A \oplus B \oplus C \oplus D\) Using Ex- OR gate only.	**7**
2	Solve the following : (i) Make a 4-input NAND gate using 2-inpur NAND gate (ii) Consider the expression \(Y = A \oplus B \oplus C\) Show that Y=1 if an odd number of variable are 1 and that Y=0 if an even number of variables are 1.	**7**
3	For the logic expression : (Y= Aar B+ar AB) (i) Obtain the truth table (ii)Name the operation performed (iii) Realize the operation using AND, OR and NOT gate. (iv) Realize the operation using only NAND gate.	**7**
4	Prove the following : (i) A positive logic AND operation is equivelnt to a negative logic OR operation and vice versa (ii) A positive logic NAND operation is equivalent to a nagative logic NOR operaion and vice versa,.	**7**

Chapter 2

1	Design a digital comparator circuit to compare two single bit numbers?	**2**
2	Give the logic equation : \(Y = ABC + B \bar CD + \bar ABC\) (i) Make a truth table (ii) Simplify using K-map (iii) Realize Y using NAND gate only	**7**
3	Give the logic equation : \(f = AB + A \bar C + AD+A \bar BC + ABC\) (i) Make a K-map for the function (ii) Express f in standard SOP form. (iii) Minimize it and realize the minimize expression using NAND gate only	**7**
4	Design a parity genrtater to generate an odd parity bit for a 4-bit word .use Ex-OR ad EX-NOR gates.	**7**

Chapter 3

1	Why decimal 6 is required to be added in BCD adder if the sum is not a valid BCD number?	**2**
2	Design a 4-bit ADDER / SUMTRACTOR circuit with ADD/SUM control line. use IC 7483 adder for the implementation.	**7**
3	Design a full adder using 8:1 multiplexer.	**7**
4	Write short notes on the following : (i) Programmable logic array (ii) programmable array logic (iii) Magnitude comparator.	**7**

Chapter 4

1	What is meant by transparent latch?	**2**
2	Design the following ripper counters using flip-flops : (i) Divide - by - 5 (ii) Divide - by- 7	**7**
3	Draw the state diagram of a modulo -4 UP/DOWN counter. Design its circuit using J-K flip-flops	**7**
4	Draw and explain bi-directional shift register in details.	**7**

Chapter 5

1	Differentiate between saturated and non-saturated logic.	**2**
2	Define the followings : (i) Propagation delay time (ii) Figure og merit (iii) Fan out and fan in (iv) Noise margin (v) Wired logic (vi) Passive pull up (vii)Active pull up	**7**
3	Explain the operation of CMOS NOR gate in detail, also explain waht happen in a CMOS gate if its output accidently gate shorted to ground ?	**7**
4	Explain the followings : (i) Why fan-out of ECL gates is higher ? (ii) Why TTL is preferred over DTL ? (iii) Why MOS logic is mainly used for LSI and VLSI applications ?	**7**