322352(28)

E. (Third Semester) Examination, Nov.-Dec., 2015

(New Scheme)

(CSE Engg. Branch)

BASIC ELECTRONICS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) of each unit is compulsory. Attempt any two questions from part (a), (b), (c) and (d) of each unit.*

Unit-I

1. (a) What is continuity equation. 2

(b) Define the term Transition capacitance of reverse biased diode and prove that :

$$C_T = \frac{C_j}{W} \quad 7$$

(c) Explain the effect of temperature on V-I characteristics of a Diode. 7

(d) Define a graded semiconductor and explain why an electric field must exist in a graded semiconductor. Prove that for an open circuited step graded P-n Junction,

$$V_0 = V_T \ln \frac{N_a N_d}{n_i^2} \quad 7$$

Unit-II

2. (a) Explain the necessity of bleeder resistor. 2

(b) With neat circuit diagram explain the working of Bridge wave rectifier. 7

(c) Explain the Zener-diode as a voltage regulator for the ckt shown in fig. a.

(i) Determine the range of R_s and I_z that will result in V_{out} being maintained at 10 V.

(ii) Determine the maximum wattage rating of the diode

(iii) If Zener maximum wattage is increased to 380 MW what is the new value of I_z min. 7

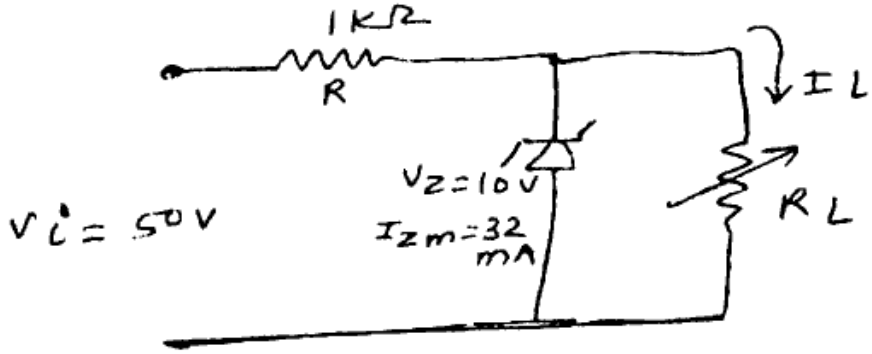


fig. a

(d) A full wave rectifier circuit is fed from a Transformer with a centre tap secondary winding. The rms voltage from either end of secondary to centre tap is 30 V. If the diode forward resistance is 2 Ω and that of half secondary is 8 Ω for a load of 1 KΩ. Calculate :

(i) Power delivered to load

(ii) Percentage regulation at full load

(iii) Efficiency of Rectification

(iv) TUF of secondary 7

Unit-III

3. (a) Draw the symbol of NPN and PNP transistors. What is the significance of the arrow in this symbol? 2

(b) Draw input and output characteristics of transistor in common base configuration. 7

(c) Explain 'Early Effect' and its 3 consequences. 7

(d) Write the Ebers-Moll equation. Sketch the circuit model which satisfies the equation and explain in brief. 7

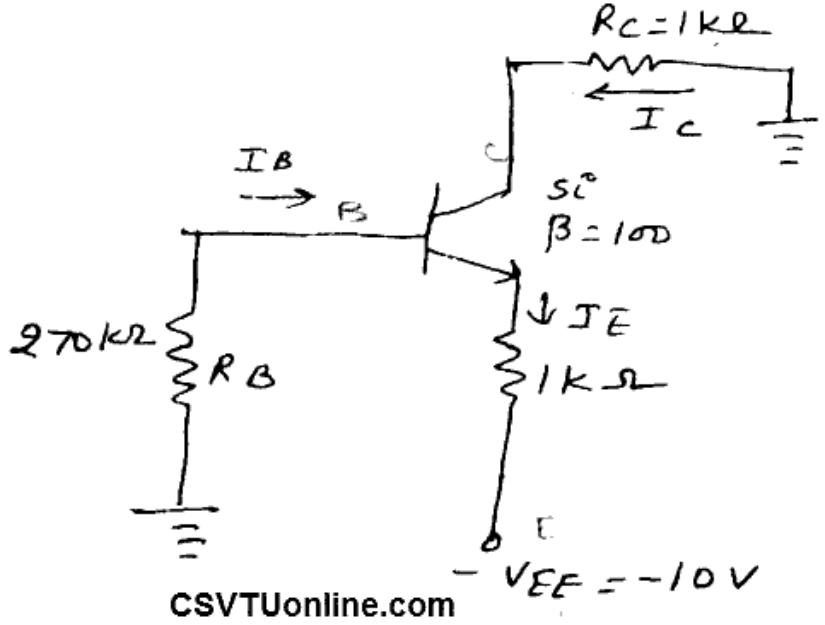
Unit-IV

4. (a) Define stability factors.

(b) Explain voltage divider biasing technique and derive expression for S, S' and S''.

(c) What do you understand by bias compensation? Explain diode compensation Technique. 7

(d) For the circuit shown in figure calculate I_B, V_C and I_{CC}. 7



Unit-V

5. (a) Define Transconductance of FET. 2

(b) Two MOSFET's having drain resistance rd_1 and rd_2 and amplification factors of μ_1 and μ_2 respectively

are connected in parallel show that

(i) $\frac{1}{rd} = \frac{1}{rd_1} + \frac{1}{rd_2}$

(ii) $\mu = \frac{\mu_1 rd_1 + \mu_2 rd_2}{rd_1 + rd_2}$ 7

(c) Draw the diagram of Enhancement type of MOSFET. Explain its construction and working 7

(d) Prove that the transconductance 9 m of a JFET is given by

$$9\,m = \frac{2}{|V_P|}\sqrt{I_{DS}\, I_{DSS}}$$

where V_P = Pinch off voltage

I_{DS} = Drain current

I_{DSS} = Maximum I_{DS} corresponding to $V_{GS} = 0$ V

| 7 |

(ii) A certain JFET has I_{DSS} 12 mA and Pinch off voltage V_p 6 Volts. Calculate the value of transconductance for V_{GS} - 1V 7