328353(28)

E. (Third Semester) Examination, April-May 2016

(New Scheme)

(Et & T Engg. Branch)

ELECTRONIC DEVICES and CIRCUITS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory. Attempt any* **two** *parts out of (b), (c) and (d). Answer should be in brief & to the points. Assume suitable data, wherever necessary.*

Unit-I

1. (a) Define Mass Action Law. 2

(b) Find the conductivity of Germanium : 7

(i) Under intrinsic conduction at 300°K.

(ii) Under acceptor impurity of 1 in 2×10^7.

Given that for Ge, n_i at 300°K is 2.5×10^{13} / cm^3 and mobility of electrons and holes are 3,800 cm^2/V-s and 1,800 cm^2/V-s respectively. Number of Ge atoms/ cm^3 = 4.4×10^{22}. 7

(c) Derive the continuity equation for holes in an elementary volume of the semiconductor. Write the corresponding continuity equation for electrons. 7

(d) Derive expression for contact difference of Potential in an open circuited step graded P-N junction. 7

Unit-II

(a) What is the feature of Ideal Diode? 2

(b) A Ge (Germanium) diode operates at a forward voltage of 0.2 volt. Calculate the factor by which the current will get multiplied when the temperature is increased from 25°C to 75°C. (assumed $n = 1$) 7

(c) A full wave P-N diode rectifier uses load resistor of $1500\ \Omega$ no filter is used. Assume each diode to have idealizied characteristic with $R_f = 12\ \Omega$ and

$R_r = \infty$. Cut in voltages may be neglected sinewave voltage applied to each diode has amplitude of 32 volts and free of 50 Hz. Calculate : 7

(i) D. C. Current

(ii) D. C. Voltage

(iii) D. C. power o/p

(iv) A. C. i/p power

(v) Rectifier efficiency

(vi) Ripple factor

(vii) Form factor

(d) What is the difference between Zener Diode & Normal Diode? Why Zener diode is preferred in voltage regulator ckt? 7

Unit-III

3. (a) Define Transistor biasing. 2

(b) Describe briefly the basic steps in the construction (fabrication) of Diffused Planar Transistor. 7

(c) In a Ge PNP transistor, the resistivities of the emitter

and base regions are respectively 4 $\Omega-\text{cm}$ and 400 $\Omega-\text{cm}$. The average time of electrons in the emitter region is $\tau_n = 1\mu s$, base width $w = 20$ Nm. Compute the approximate α of the transistor, given that D_n = 99 $\text{cm}^2/\text{V-s}$.

(d) Define the stability factor S, S^I (or S_v) and S^{II}(or S_β) and also specify the condition for avoiding thermal runaway. 7

Unit-IV

4. (a) Draw symbols & polarity conventions for n-channel JFET.

(b) An n channel FET has $a = 4 \times 10^{-4}$ cm and $N_D = 0{\cdot}8 \times 10^{15}$ electrons/cm^3. Find Pinch off voltage V_p. Given that :

$\epsilon_0 = \dfrac{1}{36\pi \times 10^9}$ F/m & relative dielectric constant of Si is 12. 7

(c) Draw & explain self bias configuration of JFET. 7

(d) Explain the following : 7

(i) Amplification factor of FET 2

(ii) FET and voltage variable resistor 5

Unit-V

5. (a) Draw symbol of N channel depletion MOSFET & P channel enhancement MOSFET. 2

(b) With the help of circuit diagram explain potential divider bias for E-MOSFET. 7

(c) Explain difference between D-MOSFET & E-MOSFET & also explain depletion MOSFET with the help of its structure, drain characteristics & transfer characteristics. 7

(d) Explain complementary MOSFET with help of its structural diagram. 7