

322352 (28)BE (3rd Semester)

Examination, Nov.-Dec., 2013

Branch : Computer Science & Engg.

BASIC ELECTRONICS (NEW)*Time Allowed : Three Hours**Maximum Marks : 80**Minimum Pass Marks : 28*

Note : Part (a) in each question is compulsory which carries two marks. Solve any two parts from part (b), (c) & (d) from each question which carries 7 marks each.

Q. 1. (a) What is continuity equation. 2

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(2)

(b) Define the term Transition capacitance of a reverse biased diode and prove that

$$C_T = \frac{\epsilon A}{W} \quad 7$$

(c) A silicon diode operates at a forward voltage of 0.45 V. Calculate the factor by which the current will be multiplied if the temperature is increased from 27°C to 152°C. 7

(d) Explain V-I characteristics of Diode in both forward bias and Reverse bias. 7

Q. 2. (a) Explain the necessity of a bleeder resistor. 2

(b) For the full-wave rectifier with a simple capacitor filter, show that the ripple factor is

$$\text{given by } r = \frac{1}{4\sqrt{3}f\epsilon R_L} \quad 7$$

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(3)

(c) With neat circuit diagram explain the working of bridge rectifier circuit.

(d) A full-wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from either end of secondary to center tap is 30 V. If the diode forward resistance is 2Ω and that of the half secondary is 8Ω , for a load of $1 \text{ k}\Omega$, calculate :

- (i) Power delivered to load
- (ii) % regulation at full load
- (iii) Efficiency of rectification
- (iv) TVF of secondary

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- Q. 3. (a) Derive relation between α and β . 2
- (b) Draw and explain input and output characteristics of a transistor in common emitter configuration. 7
- (c) Explain early effect and its consequences. 7
- (d) Write the Ebers-Moll equation sketch the circuit model which satisfies these equation and explain in brief. 7

- Q. 4. (a) Why biasing is necessary in BJT. 2
- (b) Draw the circuit diagram of a common emitter amplifier with self bias and derive the relation for stability factor. 7

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(c) What do you understand by bias compensation. Explain diode compensation techniques. 7

(d) For the circuit shown in figure 1, $I_C = 2\text{mA}$, $\beta = 100$, calculate R_E , V_{CE} and stability factor S. 7

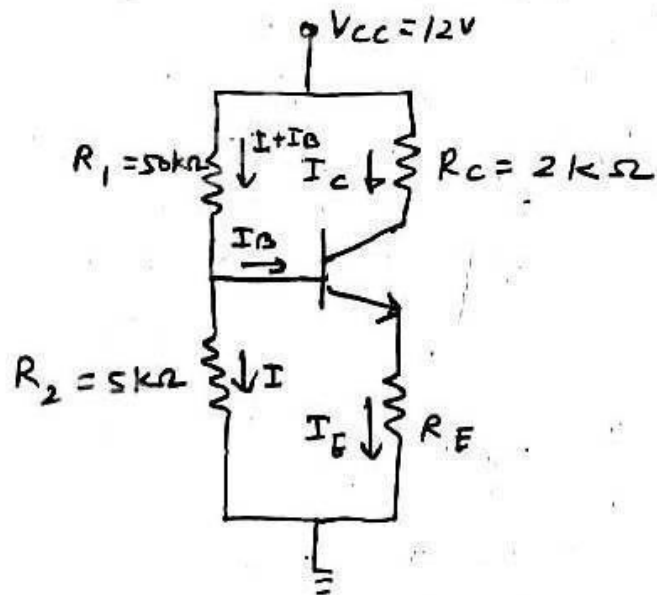


Figure 1

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(6)

- Q. 5. (a) What do you understand by "pinch off voltage" and 'cut off voltage'. 2
- (b) Differentiate between JFET and MOSFET. 7
- (c) Explain construction, working and characteristics of enhancement type MOSFET. 7
- (d) Prove that, for the JFET : 7

$$g_m = -\frac{2 I_{DSS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right]$$

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2,320