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BE (4th Semester)
Examination, Nov.-Dec., 2018
(New Scheme)

Computer Organization and Architecture

Time Allowed : 3 hours *Maximum Marks* : 80
Minimum Pass Marks : 28

Note : (*i*) Part (*a*) of each question is compulsory. Attempt any two parts from (*b*), (*c*) and (*d*).
(*ii*) The figures in the right-hand margin indicate marks.

1. (*a*) Explain the registers MBR, MAR, IR. [2]

   (*b*) Explain Von Neumann architecture with proper diagram. [7]

   (*c*) Explain bus interconnection architecture : [7]

   (*i*) Traditional Bus Architecture

   (*ii*) High Performance Architecture

   (*d*) Explain different instruction format. Draw and explain instruction execution cycle. [7]

2. (*a*) Explain DVF in division operation. [2]

   (*b*) Explain Booth's multiplication algorithm with an example. [7]

   (*c*) Explain multiplication algorithm for floating-point numbers. [7]

   (*d*) Show the content of register A, E, Q and SC during the decimal division of 1680/32. [7]

3. (*a*) What is the Control Word? [2]

   (*b*) What is a control unit? Write the function and operation of control unit. [7]

   (*c*) What are the differences between hardwired and micro-programmed control unit? [7]

   (*d*) Explain with diagram, basic organization of micro-programmed control unit. [7]

4. (*a*) What is RAM? [2]

   (*b*) What is cache coherence? Explain its solutions to solve cache coherence problem. [7]

   (*c*) Discuss memory hierarchy. Also discuss types of memory. [7]

   (*d*) Draw memory connection to CPU according to details given : [7]

   (*i*) 1 ROM 128 × 8

   (*ii*) 4 RAM 128 × 8

5. (*a*) Define Interrupt. [2]

(*b*) Explain direct memory access with proper diagram. [7]

(*c*) Explain isolated I/O configuration and memory-mapped I/O configuration. [7]

(*d*) What is pipelining? Explain linear and nonlinear pipelining. [7]

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