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328654(28)

B. E. (Sixth Semester) Examination, Nov.-Dec. 2018

(New Scheme)

VLSI DESIGN

(Branch : Et & T)

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note *: Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d).*

Unit - I

1. (a) What is the meaning of SSI, MSI and LSI? 2

   (b) Explain DC characteristics of the CMOS inverter. 7

   (c) Explain Transmission gate. Design 4 : 1 MUX with transmission gate. 7

   (d) What are the classical techniques for reducing the complexity of IC design? Explain each of them. 7

Unit - II

2. (a) What is the separator for n-type and p-type transistor in CMOS stick diagram? 2

   (b) Draw the layout of three input NAND gate by λ-rule. 7

   (c) What are the different layer representation for p-well CMOS process? 7

   (d) Draw and explain the contacts rule for CMOS. 7

Unit - III

3. (a) What is W/L ratio? 2

   (b) Draw schematic and layout of 6T SRAM cell. 7

   (c) Draw the stick diagram of JK and D flip-flop. 7

   (d) Explain CMOS stick diagram for parity generator. 7

Unit - IV

4. (a) Explain the library in VHDL. 2

   (b) Compare VLSI design style with FPGA and CPLD. 7

   (c) Explain data flow, structural and behavioural programming with example of designing of a 4 : 1 multiplexer. 7

   (d) Implement the function

   $f = x_1 x_2 x_4 + x_2 x_3 \bar{x}_4 + \bar{x}_1 \bar{x}_2 \bar{x}_3$ using two input LUT's only and explain LUT. 7

Unit - V

5. (a) What is the difference between Melay and Moore state machine? 2

   (b) Write VHDL code for Melay-type FSM for serial adder. 7

   (c) What is test bench synthesis? Write a test bench for half adder. 7

   (d) Write VHDL code for D type flip flop with synchronous and asynchronous clear. 7