

328654(28)

**BE (6th Semester)
Examination, Nov.-Dec., 2017
(New Scheme)
VLSI Design**

Time Allowed : 3 hours *Maximum Marks : 80*
Minimum Pass Marks : 28

Note : (i) Answer all questions. Part (a) is compulsory of each question. Attempt any two parts from (b), (c) and (d).
(ii) The figures in the right-hand margin indicate marks.

UNIT—I

- 1. (a) What is Moore's law ? [2]
- (b) Explain the static and dynamic power dissipation of CMOS inverter. [7]
- (c) Explain the working of NMOS inverter giving its circuit diagram and explain NMOS, NOR gate functions. [7]

- (d) What do you mean by design flow ? Find the dynamic power dissipation that results when the inverter is switched at a frequency of 2MHz. The CMOS inverter is loaded by a 15pF capacitance with supply $V_{DD} = 5V$. [7]

UNIT—II

- 2. (a) What do you mean by Bi-CMOS transistor ? Give at least one advantage. [2]
- (b) Write short notes on AOI (AND-OR-INVERT) and OAI (OR-AND-INVERT) CMOS Gate. [7]
- (c) Explain and draw the different steps for CMOS SOI. [7]
- (d) What is Euler graph ? Explain with suitable example. http://www.csvtuonline.com [7]

UNIT—III

- 3. (a) What are combinational circuits ? [2]
- (b) Explain in brief with working of three-transistor DRAM cell layout. [7]
- (c) What do you mean by Flip-Flop ? Explain with detailed layout of J-K Flip-Flop. [7]
- (d) What are parity generator and ratioed logic ? Explain in brief. [7]

UNIT—IV

- 4. (a) What is Programmable Array Logic (PAL) ? [2]

(3)

- (b) Explain behavioral style of modeling in brief with example. [7]
- (c) What do you mean by VHDL? Write a VHDL source code for 4-bit adder. [7]
- (d) Compare VLSI design style with FPGA and CPLD. [7]

UNIT—V

- 5. (a) Give the features of sequential circuits. [2]
- (b) Write down VHDL code for FSM of BCD counter by Moore machine. [7]
- (c) Write short notes on any one of the following : [7]
 - (i) Delay models of VHDL
 - (ii) Operator overloading
- (d) Write a VHDL program to design D-flip flop with synchronous and asynchronous. [7]

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