Printed Pages: 3

Roll No.

328613(28)

BE (6th Semester) Examination, April-May, 2018

(Old Scheme)

Advanced Microprocessor & Interfacing

Time Allowed: 3 hours

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Maximum Marks: 80

Minimum Pass Marks: 28

Note: Part (a) is compulsory which carries 2 marks and solve any two parts from (b), (c) and (d) carry 7 marks each.

- 1. (a) What do you understand by PSW in 8086?
 - (b) Explain addressing modes in 8086.
 - (c) Explain the interrupt execution with the help of an example using interrupt instructions.
 - (d) Why segmented memory is used in 8086? What are its advantages?
- 2. (a) What is the job of MN / $M\overline{X}$ pin in 8086?
 - (b) Explain interrupt priority management.

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- (c) Discuss read and write operation in minimum mode with the help of the timing diagram.
- (d) Interface two 4K×8 EPROM's and two 4K×8 RAM chips with 8086 and select suitable maps.

Range: EPROM → FE000H to FFFFFH

RAM → FC000H to FDFFFH

- 3. (a) Differentiate between 8259 and 8259A.
 - (b) Explain the internal architecture of 8257 DMA controller in detail.
 - (c) Explain the interfacing of 8255A with an A/D and D/A subsystem.
 - (d) Explain the following signal description of 8251: http://www.csvtuonline.com

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- (i) C/\bar{D}
- (ii) TxE
- (iii) SYNDET
- (iv) DTR
- (v) RTS

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- 4. (a) What do you mean by exception?
 - (b) Explain register set of 80386.
 - (c) Discuss real and protected mode in 80386.
 - (d) Describe 80486 internal architecture.

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(Turn Over)

(Continued)

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- 5. (a) What do you mean by a multiprocessor system?
 - (b) Explain data types and data formats of 8087 math coprocessor.
 - (c) Explain IOP architecture.
 - (d) How CPU communicates with IOP?

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